CLAIMS

1. A method of manufacturing a semiconductor device comprising:

forming a silicide layer having an NiSi phase on source and drain regions in a semiconductor substrate, where the junction depth of the source and drain regions is from 20 nm to 60 nm below the lower surface of the silicide layer; and

after the formation of the silicide layer having the NiSi phase, performing manufacturing steps at a temperature not exceeding a critical temperature Tc, which meets the following expression:

$$Tc = a \times Dj + b,$$

where $a = 6.11\ (20 < Dj \leq 26)$

$= 1.60\ (26 < Dj \leq 60)$,

$b = 290.74\ (20 < Dj \leq 26)$

$= 408\ (26 < Dj \leq 60)$,

Dj is a junction depth (nm) measured from the lower surface of the silicide layer, and Tc is a critical temperature (°C) during a heat treatment.

2. The method of manufacturing a semiconductor device according to claim 1, wherein after the formation of the silicide layer having the NiSi phase, a silicon nitride layer is deposited so as to cover the silicide layer.

3. The method of manufacturing a semiconductor device according to claim 2, wherein an insulating layer is formed on the silicon nitride layer, and the insulating layer and the silicon nitride layer are selectively etched and removed by an RIE method so as to form openings reaching the source and drain regions through the insulating layer and the silicon nitride layer.

4. The method of manufacturing a semiconductor device according to claim 1, wherein an insulating layer is formed on the silicide layer having the NiSi phase, an opening reaching the silicide layer having the NiSi phase is formed through the insulating layer, and the opening is filled with copper by a coating method, thereby forming an electrode.

5. The method of manufacturing a semiconductor device according to claim 4, wherein before copper is filled in the opening, an inside of the opening is subjected to a plasma containing NF_3, and then a barrier metal layer is formed over an interior of the opening including a bottom portion thereof by a sputtering method without subjecting the inside of the opening to the atmosphere.

6. A semiconductor device comprising a semiconductor element including:

a gate electrode formed on a silicon semiconductor substrate;

source and drain regions formed at both sides of the gate electrode in the silicon semiconductor substrate; and

an NiSi layer formed on the source and drain regions,

where a junction depth of the source and drain regions being from 20 nm to 60 nm from a lower surface of the NiSi layer, Ni atoms existing in the source and drain regions, and a concentration of the Ni atoms at the junction depth being at 1.6×10^{14} cm^{-3} or less.

7. The semiconductor device according to claim 6, wherein the concentration of the Ni atoms in the silicon semiconductor substrate at a portion 10 nm in depth from the lower surface of the NiSi layer is at 5×10^{18} cm^{-3} or more, and 3×10^{21} cm^{-3} or less.

8. The semiconductor device according to claim 6, further comprising a silicon nitride layer formed to cover the NiSi layer and to have an optical refractive index of 1.89 or less.

9. The semiconductor device according to claim 6, further comprising an insulating layer formed on the NiSi layer, and an electrode of a metal material containing copper formed in the insulating layer for being electrically in contact with the NiSi layer.

10. The semiconductor device according to claim 6, wherein the gate electrode is completely formed of the NiSi layer.

11. The semiconductor device according to claim 6, wherein a plurality of the semiconductor elements are formed on the silicon semiconductor substrate, each being isolated by an insulating layer filling up shallow trenches formed in the silicon semiconductor substrate.

12. The semiconductor device according to claim 11, wherein n-type MOSFETs and p-type MOSFETs constituting a logic circuit.

13. The semiconductor device according to claim 7, further comprising a silicon nitride layer formed to cover the NiSi layer and to have an optical refractive index of 1.89 or less.

14. The semiconductor device according to claim 7, further comprising an insulating layer formed on the NiSi layer, and an electrode of a metal material containing copper formed in the insulating layer for being electrically in contact with the NiSi layer.

15. The semiconductor device according to claim 7, wherein the gate electrode is completely formed of the NiSi layer.

16 The semiconductor device according to claim 7, wherein a plurality of the semiconductor elements are formed on the silicon semiconductor substrate, each being isolated by an insulating layer filling up shallow trenches formed in the silicon semiconductor substrate.

17. The semiconductor device according to claim 16, wherein n-type MOSFETs and p-type MOSFETs constituting a logic circuit.

18. The semiconductor device according to claim 6, further comprising an insulating layer having a dielectric constant of 3.9 or more between the gate electrode and the silicon semiconductor substrate.

19. The semiconductor device according to claim 7, further comprising an insulating layer having a dielectric constant of 3.9 or more between the gate electrode and the silicon semiconductor substrate.